CLAIMS:

1. An information storage process, including applying pressure to and removing pressure from one or more regions of a substance to store information in said one or more regions.

2. A process as claimed in claim 1, wherein said one or more regions provide one or more memory cells for a memory device.

3. A process as claimed in claim 2, wherein dimensions of each of said memory cells are on a nanometer scale.

4. A process as claimed in claim 1, including measuring a property of said one or more regions to determine the information stored in said one or more regions.

5. A process as claimed in claim 4, wherein said property includes conductivity or resistance.

6. A process as claimed in claim 1, wherein the applying and removing of pressure includes transforming said one or more regions from at least one first phase to at least one second phase.

7. A process as claimed in claim 6, wherein said at least one first phase includes an amorphous phase, and said at least one second phase includes at least one crystalline phase.

8. A process as claimed in claim 7, wherein said amorphous phase is a relaxed amorphous phase.

9. A process as claimed in claim 8, wherein said substance is substantially silicon.

10. A process as claimed in claim 6, including heating said one or more regions to induce further phase change in said one or more regions.

11. A process as claimed in claim 10, wherein said heating transforms said at least one crystalline phase to a more conductive crystalline phase.

12. A process as claimed in claim 1, wherein the step of applying and removing pressure includes controlling at least one of the applying and removing of pressure to determine the information stored in said one or more regions.

13. A process as claimed in claim 1, wherein the applying and removing of pressure includes controlling a rate of said removing of pressure to determine the information stored in said one or more regions.

14. A process as claimed in claim 1, including selecting the pressure applied to each of said one or more regions to determine the information stored in said one or more regions.

15. A process as claimed in claim 14, wherein the pressure is selected from a plurality of predetermined pressures to provide multi-bit information storage in each of said one or more regions.

16. A process as claimed in claim 1, wherein the applying and removing of pressure changes the electrical conductivity of said one or more regions from a first electrical conductivity to a second electrical conductivity, and the process further includes applying pressure to and removing pressure from said one or more regions to change the electrical conductivity of said one or more regions from said second electrical conductivity to a third electrical conductivity.

17. A process as claimed in claim 16, wherein said third electrical conductivity is substantially equal to said first electrical conductivity.

18. A process, including applying pressure to and removing pressure from one or more regions of relaxed amorphous silicon to transform said one or more regions into substantially crystalline silicon.

19. A process as claimed in claim 18, including the further step of heating said one or more regions to transform the substantially crystalline silicon to a further crystalline phase.

20. A process as claimed in claim 19, wherein the further crystalline phase is more electrically conductive than the substantially crystalline silicon.

21. A process as claimed in claim 18, including the further step of applying pressure to and removing pressure from said one or more regions to transform the substantially crystalline silicon in said one or more regions into substantially amorphous silicon.

22. A process as claimed in claim 18, including controlling the pressure applied to the one or more regions to determine at least one dimension of the one or more substantially crystalline silicon regions.

23. A process as claimed in claim 22, wherein the pressure applied to each region is selected from a plurality of predetermined pressures.

24. A process as claimed in claim 22, including controlling the further application of pressure to and removal of pressure from said one or more regions to change said at least one dimension of the substantially crystalline silicon regions.

25. A process, including applying pressure to and removing pressure from one or more regions of a substance to change at least one property of said one or more regions.

26. A process as claimed in claim 25, wherein said at least one property includes an electrical property.

27. A process, including applying pressure to and removing pressure from one or more regions of a substance to induce a phase change in at least a portion of each of said one or more regions.

28. A process as claimed in claim 27, including heating said one or more regions to induce further phase change in said one or more regions.

29. A process, including applying pressure to and removing pressure from one or more regions of relaxed amorphous silicon to transform at least a portion of each of said one or more regions to at least one crystalline phase.

30. A process as claimed in claim 29, including heating said one or more regions to transform the at least one crystalline phase to a further crystalline phase.

31. A process as claimed in claim 29, including heating said one or more regions to transform the at least one crystalline phase and any untransformed amorphous silicon in said one or more regions to a further crystalline phase.

32. A process as claimed in claim 29, including applying pressure to and removing pressure from the one or more regions to transform the at least one crystalline phase to an amorphous phase.

33. A process for producing regions of substantially crystalline and substantially amorphous silicon by applying pressure to and removing pressure from one or more regions of a substantially silicon substrate.

34. A process for producing regions having different electrical and/or physical properties by applying pressure to and removing pressure from one or more regions of a substantially silicon substrate.

35. The present invention also provides a device having components for executing the steps of any one of claims 1 to 34.

36. The present invention also provides a structure produced by executing the steps of any one of claims 1 to 34.

37. A memory device, including a plurality of memory cells created by applying pressure to and removing pressure from one or more regions of a substance to change the electrical conductivity of said one or more regions from a first electrical conductivity to a second electrical conductivity to provide said plurality of memory cells.

38. A memory device as claimed in claim 37, wherein dimensions of said memory cells are on a nanometer scale.

39. A memory device, including a plurality of substantially conducting regions of crystalline silicon in a layer of substantially insulating relaxed amorphous silicon.

40. A memory device, including a plurality of first regions having a first electrical conductivity, a plurality of second regions having a second electrical conductivity, and at least one electrically conductive probe for determining the conductivities of said regions to determine stored information represented by said conductivities.

41. A memory device as claimed in claim 40, wherein said at least one electrically conductive probe is adapted to apply pressure to and remove pressure from selected ones of said regions to change the electrical conductivity of the selected regions and thereby to store or erase information.

42. A memory device as claimed in claim 40, including a movable support for translating said at least one electrically conductive probe to access selected regions of said device.

43. A memory device as claimed in claim 40, including at least one transforming probe adapted to apply pressure to and remove pressure from selected ones of said regions to change the electrical conductivity of the selected regions and thereby to store or erase information.

44. A memory device as claimed in claim 43, including a movable support for translating said at least one transforming probe to access said selected regions.

45. A memory device, including a plurality of first regions having a first electrical conductivity as a result of applying pressure to and removing pressure from said first regions, a plurality of second regions having a second electrical conductivity, conductive wordlines adjacent said first regions and said second regions, and conductive bitlines adjacent said first regions and said second regions; wherein the conductivity of a selected one of said first regions and said second regions can be determined by accessing a corresponding wordline and a corresponding bitline.

46. A memory device, including a plurality of substantially insulating regions of amorphous silicon in a layer of conducting crystalline silicon, said regions of amorphous silicon formed by applying pressure to and removing pressure from corresponding regions of said layer of conducting crystalline silicon.

47. A memory device adapted to store information in memory cells of said device by changing an electrical property of silicon.

48. A memory device, including at least one indenter tip for storing and/or erasing information in cells of said device by indentation.

49. A structured material, including one or more substantially crystalline regions in a layer of relaxed amorphous silicon.